

**ADVANCED ADAPTIVE PRE-DISTORTION IN A
RADIO FREQUENCY TRANSMITTER**

Related Application

5 This application claims the benefit under 35 U.S.C. § 119(e) of U.S. Provisional Application No. 60/178,207, filed January 26, 2000, the disclosure of which is hereby incorporated by reference.

Background of the Invention

10 Field of the Invention

 The present invention is generally related to communications systems. In particular, the present invention relates to linearizing Radio Frequency (RF) power amplifiers.

15 Description of the Related Art

 Radio Frequency (RF) power amplifiers prepare a signal for transmission by increasing the power of the signal. The signal, such as a television signal, radio signal, or cell phone signal, can be transmitted through the air via an antenna. Other signals, such as those found in cable-TV systems, are transmitted through cables.

20 One class of RF power amplifiers is known as Class A. Class A amplifiers exhibit good intrinsic linearity but are relatively inefficient. A Class A amplifier can exhibit an efficiency as low as 1%. The efficiency is low because only a small portion of the potential output capability of a Class A amplifier can be used in order to maintain the operation of the amplifier in a linear region. When the overall power output is
25 relatively high, a Class A amplifier can waste a lot of power and in turn, require bulky and expensive thermal management techniques to remove the excess heat generated.

 Other classes of RF power amplifiers, such as Class AB, Class B, Class C, etc., are more efficient than a Class A amplifier, but are also intrinsically less linear. Non-linear amplification introduces distortion to the amplified RF signal. The distortion can
30 manifest itself by harmonic frequencies and intermodulation.

Conventional methods attempt to correct the non-linearities of a nonlinear RF power amplifier by introducing Cartesian feedback, feedforward compensation, and predistortion techniques.

5 Cartesian feedback applies negative feedback to an RF transmitter, which includes an RF amplifier. A sample of the output of the RF amplifier is demodulated and fed back to the input of the transmitter. A disadvantage of Cartesian feedback, as a form of closed loop negative feedback, is that it must be unconditionally stable. Given the delay encountered in modulation and demodulation, the stability requirement gives rise to a relatively narrow operating bandwidth that is impractical for modern wideband
10 code division multiple access (W-CDMA) cellular systems.

Feedforward is a technique in which an additional linear amplifier subtracts the artifacts of nonlinearity from the RF amplifier such that the RF transmitter produces a linearized output. An error signal is derived from comparison of the input to the RF amplifier and the output of the RF amplifier. The input to the RF amplifier is delayed to
15 compensate for the delay through the RF amplifier. The error signal is then amplified by the additional linear amplifier and combined with a delayed output of the RF amplifier to reduce the distortion of the RF amplifier. The output of the RF amplifier is delayed prior to the subtraction in order to compensate for the delay encountered by the error signal through the additional linear amplifier. Feedforward techniques are open
20 loop by nature and can operate over a relatively wide bandwidth. However, the matching of the delays through the RF power amplifier and the additional linear amplifier can be difficult to implement in practice. A mismatch in either or both of the delays seriously undermines the effectiveness of the distortion cancellation.

Predistortion is another conventional technique used to enhance the linearity of a
25 nonlinear amplifier. A digital signal processor (DSP) predistorts the input signal by reference to a predistortion kernel with a complement of the expected distortion of the nonlinear amplifier.

A form of predistortion known as adaptive predistortion further enhances the effectiveness of predistortion by monitoring the output of the RF amplifier and updating
30 the coefficients used by the DSP. A sample of the output of the RF amplifier is demodulated to baseband, and the baseband signal is analog-to-digital converted and

applied to the DSP as an input. One disadvantage to present techniques of adaptive predistortion is the relatively limited range and relatively expensive cost of the analog-to-digital converter (ADC). The relatively limited dynamic range of the ADC limits the ability for adaptive predistortion techniques to cancel out nonlinearities.

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Summary of the Invention

The present invention solves these and other problems by providing adaptive predistortion circuits that efficiently use the dynamic range of an analog-to-digital converter (ADC) used to sample the distortion of an RF transmitter. A main signal component of a down-converted output of the RF transmitter is removed prior to the analog-to-digital conversion, thereby allowing relatively more of the input range of the analog-to-digital converter to capture the error signal within the down-converted output. Embodiments of the present invention can thereby adaptively tune the predistortion stage to a higher degree of linearity or can use lower cost analog-to-digital converters with fewer quantization steps for the same performance.

An embodiment of the present invention includes an RF transmitter whose input is adaptively predistorted in a complementary manner to the RF transmitter's intrinsic distortion to reduce the distortion in the output of the RF transmitter. Coefficients of the predistortion process are updated while the RF transmitter is operating to adaptively linearize the transmitter's output. A sample of the output of the RF transmitter is down-converted and combined with a delayed version of the input reference signal. The delayed version of the input reference signal can additionally be phase rotated and amplitude scaled such that the delayed version of the input reference signal further reduces a main signal component of the down-converted sample when the down-converted sample and the delayed version of the input reference signal are combined.

In a conventional system, the down-converted sample is converted by an analog-to-digital converter. As the main signal component is a substantial component of the magnitude of the down-converted sample, conventional systems do not fully utilize the dynamic range of the analog-to-digital converter to capture the error component of the down-converted sample.

10 In an embodiment according to the present invention, the combining of the
down-converted sample with the delayed version of the input reference signal
substantially reduces the main signal component of the combined signal while
substantially maintaining the error component of the down-converted sample, thereby
5 allowing an analog-to-digital converter to more accurately capture the error component.
The combined signal advantageously allows the analog-to-digital converter to capture
the error components in smaller and more precise quantization steps and can enhance
the adaptive updates to the predistortion and thereby enhance the improvement to
linearity of the predistortion, or allow the cost effective use of a simpler and cheaper
10 analog-to-digital converter with fewer bits.

15 One embodiment of the present invention further adaptively updates the delay,
phase rotation, and amplitude scaling of the delayed input signal to improve the
cancellation of the main signal component by the delayed input signal. One algorithm
that adaptively tunes the delay, phase rotation, and amplitude scaling, seeks to decrease
the power of the combined signal.

20 Embodiments of the present invention can be utilized with transmitters that
directly up-convert from baseband to RF and transmitters that modulate data on an
Intermediate Frequency (IF) that is subsequently up-converted to RF. One embodiment
according to the present invention down-converts the RF to IF, and then demodulates
the IF to complex baseband, by, for example, digital quadrature conversion. Another
embodiment directly down-converts the RF to complex baseband.

25 In one embodiment, the predistortion circuit is implemented with dedicated
hardware and predistortion kernels, and the predistortion circuit receives updates from a
microprocessor to adaptively configure the predistortion characteristic to time-varying
conditions of the transmitter. A complex finite impulse response (FIR) filter delays the
input signal and can further rotate the phase and scale the magnitude of the delayed
input signal. The complex FIR filter can be further configured to receive updates from
the microprocessor to adaptively cancel the main signal component with the delayed
input signal.

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Brief Description of the Drawings

These and other features of the invention will now be described with reference to the drawings summarized below. These drawings and the associated description are provided to illustrate preferred embodiments of the invention, and not to limit the scope of the invention.

Figure 1 illustrates a block diagram of an RF transmitter according to a conventional Adaptive Predistortion Linearization technique.

Figure 2 illustrates a Power Spectral Density plot of the RF transmitter according to the conventional Adaptive Predistortion Linearization technique.

Figure 3 illustrates a block diagram of an embodiment of an RF transmitter according to the present invention.

Figure 4 illustrates an embodiment of an RF transmitter according to the present invention.

Detailed Description of the Preferred Embodiments

Although this invention will be described in terms of certain preferred embodiments, other embodiments that are apparent to those of ordinary skill in the art, including embodiments which do not provide all of the benefits and features set forth herein, are also within the scope of this invention. Accordingly, the scope of the present invention is defined only by reference to the appended claims.

Embodiments of the present invention advantageously allow the efficient use of the dynamic range of an analog-to-digital converter (ADC) used to sample the output signal in an RF transmitter with an adaptive predistortion linearization circuit. In one embodiment, the efficient use of the dynamic range of the ADC enhances the linearity of the RF transmitter. In another embodiment, the efficient use of the dynamic range of the ADC allows a substitution of a less expensive ADC with no decrease in performance. These two benefits can be appropriately combined to achieve a desired cost/performance tradeoff.

Figure 1 illustrates a block diagram of a conventional RF transmitter 100 with adaptive predistortion. The RF transmitter 100 is part analog and part digital. Line 110 indicates the division between the analog portion and the digital portion. The RF

transmitter 100 receives a digital input signal, $V_m(t)$ 112. As shown in Figure 1, the input signal 112 is already modulated with, for example, code division multiple access (CDMA). The input signal 112 is applied to a digital compensation signal processing (DCSP) circuit 114. The DCSP circuit 114 predistorts the input signal 112 such that after amplification, the output of the RF transmitter 100 is less distorted. The DCSP circuit 114 references a predistortion kernel to determine how to predistort the input signal 112. As will be explained later, the coefficients of the predistortion kernel can be adjusted to account for time-varying nonlinearities.

A predistorted output signal 116 of the DCSP circuit 114 is applied to a digital-to-analog converter 118, which converts the predistorted output signal 116 of the DCSP circuit 114 to a predistorted analog signal 120. Typically, the predistorted analog signal 120 is an intermediate frequency (IF) signal or complex baseband. An RF up-converter 122 mixes the predistorted analog signal 120 with a local oscillator to produce a modulated carrier wave termed a low power RF signal 124. The low power RF signal 124 is amplified by an RF amplifier 126 to a high power RF signal 128.

The nonlinearities of the RF amplifier 126 are corrected by the DCSP circuit 114 such that the high power RF signal 128 exhibits relatively low distortion. A coupler 130, such as a Lange, a Hybrid, or a Quadrature coupler, provides an RF sample 132 of the high power RF signal 128.

An RF down-converter 134 converts the RF sample 132 down from a radio frequency signal to a down-converted signal 136, which is a relatively lower frequency. In one embodiment, the down-converted signal 136 is complex baseband. In another embodiment, the down-converted signal 136 is an IF signal. An analog-to-digital converter 138 converts the analog down-converted signal 136 to a digital feedback signal 140.

Typically, the down-converted signal 136, which is converted by the analog-to-digital converter 138, remains a relatively high bandwidth signal. In one embodiment, the down-converted signal 136 is converted by a relatively high-speed pipeline analog-to-digital converter (ADC), such as an AD9432 available from Analog Devices, Inc. In another embodiment, the down-converted signal 136 is converted by a Flash ADC.

High-speed ADCs are relatively limited in dynamic range and become progressively more expensive as the dynamic range of the ADC increases.

The limited dynamic range of the high-speed ADCs used to monitor the down-converted signal 136 is a source of a problem. The RF sample 132 and the down-converted signal 136 contain at least one main signal, and further contain distortion artifacts of the main signal.

Figure 2 is a power spectral density plot 200 of test results of conventional systems and one embodiment according to the present invention. The test were conducted with an amplifier input signal conforming to a 1900-megahertz (MHz) wideband CDMA signal, which is representative of a personal communication service (PCS) cellular communications signal. For clarity, the power density plot 200 is normalized over frequency.

As shown in Figure 2, a main signal component 210 is much higher in magnitude than an intrinsic distortion 220 of the RF amplifier 126, i.e., the distortion artifacts 220 without predistortion linearization. The main signal component 210 is even higher in magnitude than a distortion 230 of the RF amplifier 126 with conventional predistortion linearization. For example, where the RF amplifier 126 is a Class AB RF power amplifier, the distortion and nonlinear artifacts can be buried 40 decibels (dB) below the main output signal.

When the analog-to-digital converter 138 monitors the down-converted signal 136, much of the dynamic range of the analog-to-digital converter 138 is used to accommodate the main output component 210 of the down-converted signal 136. As a result, only a relatively small portion of the ADC's dynamic range is used to quantize the error signal. Thus, conventional adaptive predistortion techniques rely upon relatively expensive ADCs with large dynamic ranges and yet, conventional adaptive predistortion techniques exhibit a relatively low sensitivity to the nonlinearity components of the RF output.

In a sample calculation, the dynamic range of a typical linear ADC is approximately 6 dB per bit, and a 10-bit and a 12-bit ADC exhibit approximately a 60-dB and a 72-dB dynamic range, respectively. Since approximately 40 dB of the dynamic range of the ADC is consumed by the main signal, only approximately 20 dB

and 32 dB, respectively, of the dynamic range of the ADC remains for the error component. Thus, the error component is effectively converted by only 3 and 5 bits, respectively, of the 10-bit and the 12-bit ADCs.

Embodiments of the present invention advantageously cancel or filter a substantial portion of the main output signal from the down-converted signal 136 or digital baseband. By canceling or filtering at least a portion of the main output signal from the down-converted signal 136, embodiments of the present invention can advantageously convert the error signal with greater sensitivity. In one embodiment, the enhanced sensitivity allows a reduction of distortion, as shown by an improved correction 240 in Figure 2.

Further details of embodiments of the present invention, which advantageously utilize the dynamic range of the analog-to-digital converter 138 more efficiently than conventional systems, will be described later in connection with Figures 3 and 4.

As further illustrated by Figure 1, the digital feedback signal 140 is applied to an adaptive control processing and compensation estimator (ACPCE) circuit 142. The ACPCE circuit 142 compares the input signal 112 to the digital feedback signal 140. The ACPCE appropriately delays the input signal 112 to account for the delay of the digital feedback signal 140 through a first path 144. The ACPCE circuit 142 also scales the input signal 112 or the digital feedback signal 140 to account for the variations in gain encountered through amplification, coupling, and conversion stages.

Based on the computed difference between the input signal 112 and the digital feedback signal 140, the ACPCE circuit 142 updates the DCSP 114 via a state parameter update vector 146. The state parameter update vector 146 updates the predistortion kernel in the DCSP 114 and enhances the linearity correction of the DCSP 114.

Figure 3 illustrates a block diagram of an embodiment of an RF transmitter 300 according to the present invention. The RF transmitter 300 is again a mixed analog and digital system, where line 310 indicates the division between the analog portion and the digital portion of the RF transmitter 300.

The RF transmitter 300 receives the digital input signal, $V_m(t)$ 112. As shown in Figure 3, the input signal 112 is already modulated with, for example, CDMA. The

input signal 112 is applied to the DCSP circuit 114, which predistorts the input signal 112 to improve the linearity of the output of the RF transmitter 300. The DCSP circuit 114 references an internal predistortion kernel to determine how to predistort the input signal 112.

5 The input signal 112 is also applied to an adaptive control processing and compensation estimator (ACPCE) circuit 312 and a complex finite impulse response (FIR) filter 314. The ACPCE 312 and the complex FIR 314 filter will be described in greater detail later.

10 As described in connection with Figure 1, the predistorted output signal 116 of the DCSP circuit 114 is applied to the digital-to-analog converter 118, which converts the predistorted output signal 116 of the DCSP circuit 114 to a predistorted analog signal 120. In one embodiment, the digital-to-analog converter 118 is an AD9772, which is available from Analog Devices, Inc. The RF transmitter 300 further includes a first reconstruction filter 316, which is a low pass filter that removes the quantization
15 noise and higher Nyquist images from the output of the digital-to-analog converter 118. A reconstructed output 318 is applied to the RF up-converter 122, which mixes the reconstructed output 318 with a local oscillator to produce the carrier wave low power RF signal 124.

20 Of course, the DCSP circuit 114 can generate separate I and Q signals for phase modulated symbols and the digital-to-analog converter 118 can include separate converters for the I and Q signals, which are later combined in the RF up-converter 122. In another embodiment, the RF up-converter 122 further includes a modulator circuit and operates as a direct up-converter, thereby directly receiving the digital IF or I-Q data and transforming the data to the digital symbols as specified by the modulation
25 scheme.

 The low power RF signal 124 is amplified by the RF amplifier 126 to the high power RF signal 128. The RF outputs of several RF up-converters and of various modulation schemes can be combined and amplified by the RF amplifier 126 of the RF transmitter 300.

30 The nonlinear behavior of the RF amplifier 126 distorts the predistorted low power RF signal 124 such that the high power RF signal 128 exhibits relatively low

distortion. The path from the input signal 112 to the high power RF signal 128 is referred to as a forward transmitting path 320.

The coupler 130 provides the RF down-converter 134 with the RF sample 132 of the high power RF signal 128. The RF down-converter 134 converts the RF sample 132 down from radio frequency to the down-converted signal 136, which is a relatively lower frequency. The path from the high power RF signal 128 to the down-converted signal 136 is referred to as a return path 322.

The down-converted signal 136 is advantageously combined at a node 332 with a delayed version of the input signal 324. The combination of the down-converted signal 136 with the delayed version of the input signal 324 increases the proportion of error components to main signal components in the analog domain to improve the efficiency with which an input range of an analog-to-digital converter (ADC) 344 detects the error components within the high power RF signal 128.

The input signal 112 passes through the complex FIR filter 314, a second digital-to-analog converter 326, and a second reconstruction filter 328, to become the delayed version of the input signal 324. The path from the input signal 112 to the delayed version of the input signal 324 is termed a side path 330.

The complex FIR filter 314 converts the input signal 112 to a delayed input signal 334. The delayed input signal 334 is delayed by the complex FIR filter 314 such that the delay of the side path 330 is approximately equal to the sum of the delays of the forward transmitting path 320 and the return path 322. The complex FIR filter 314 can further adjust the relative gain (or loss) and rotate the relative phase between the input signal 112 and the delayed input signal 334. A feedback state vector 336 from the ACPCE 312 provides the parameters for the adjustment and will be described in greater detail later. In another embodiment, the complex FIR filter 314 is instead, an infinite impulse response (IIR) filter.

The delayed input signal 334 is applied to the second digital-to-analog converter 326 and converted to analog form. In one embodiment, the second digital-to-analog converter 326 is an AD9772. The analog output 338 of the second digital-to-analog converter 326 is low pass filtered by the second reconstruction filter 328 to remove

quantization noise and higher Nyquist images. The delayed version of the input signal 324 is the output of the second reconstruction filter 328.

The node 332 subtracts the delayed version of the input signal 324 from the down-converted signal 136, thereby advantageously canceling or filtering a substantial portion of a main signal component of the down-converted signal 136. It will be understood by one of ordinary skill in the art that the node 332 can be a summing node, where one of a main signal component of the delayed version of the input signal 324 or a main signal component of the down-converted signal 136 is the inverse of the other. In one embodiment, the summing node is an active op-amp summing junction. In another embodiment, the summing node is a resistive summing circuit. The output of the node is an error signal 338. Where the error signal 338 is defined as $V_e(t)$, the down-converted signal 136 as $V_f(t)$, and the delayed version of the input signal 324 as $V_{dm}(t)$, the node performs the following computation:

$$V_e(t) = V_f(t) - V_{dm}(t)$$

An anti-aliasing filter 340 low pass filters the error signal 338 and can further include a gain stage to conform a filtered output 342 of the anti-aliasing filter 340 to the input range of the ADC 344. The filtered output 342 is then converted to digital by the ADC 344. Advantageously, the main signal component of the down-converted signal 136 can be reduced by the subtraction with the delayed version of the input signal 324. As described in connection with Figure 1, the main signal dominates the magnitude of the down-converted signal 136. Of course, as the magnitude of the down-converted signal 136 decreases, the gain stage within the anti-aliasing filter 340 can increase the magnitude of the filtered output 342 to conform the magnitude of the filtered output 342 to the input range of the ADC 344.

By separating the main signal component from the down-converted signal 136 through subtraction with the delayed version of the input signal 324, the input range of the ADC 344 can be more fully utilized. For example, where the main signal component is substantially removed from the down-converted signal 136, the error signal 338 corresponds substantially to the error signal component of the down-converted signal 136. Thus, nearly the full range of the ADC 344 measures the error component of the down-converted signal 136.

By contrast, in the conventional RF transmitter with adaptive predistortion as described in connection with Figure 1, the entire down-converted signal 136, represented above as $V_f(t)$, is converted by the analog-to-digital converter 138. As described in connection with Figure 1, the main signal dominates the magnitude of the down-converted signal 136, leaving only a few bits to quantize the error signal within the down-converted signal 136.

Returning to Figure 3, a digital error signal 346 from the ADC 344 is applied to the ACPCE 312. Based on the content of the digital error signal 346, the ACPCE 312 can update the coefficients of the DCSP 114 through the digital feedback signal 140 to improve the predistortion characteristics of the DCSP 114 and thereby reduce the nonlinearity in the high power RF signal 128.

In one embodiment, the ACPCE 312 can also adaptively update the coefficients of the complex FIR filter 314 through the feedback state vector 336 to adjust the combination of the delayed version of the input signal 324 with the down-converted signal 136 at the node 332. The ACPCE 312 can adjust the delay, magnitude, and phase rotation of the complex FIR filter 314. One algorithm that can be used by the ACPCE 312 is to monitor the digital error signal 346 and adjust the delay, magnitude, and phase rotation of the complex FIR filter 314 to minimize power in the digital error signal 346. It will be understood by one of ordinary skill in the art that other components can be used to implement delays, magnitude adjustments, and phase rotations. For example, shift registers and dual port RAMs can implement delays. The magnitude adjustment and the phase rotations can be implemented with analog circuits.

Figure 4 illustrates another embodiment of an RF transmitter 400 according to the present invention. The RF transmitter 400 includes a signal processor 402, which implements the functions of the DCSP 114 and the complex FIR 314 described in connection with Figure 3. The signal processor 402 is preferably implemented in dedicated hardware such as a custom application specific integrated circuit (ASIC) or a field programmable gate array (FPGA) so that the signal processor 402 can respond to a high data transfer rate in real time. Suitable FPGAs are available from vendors such as Xilinx, Inc.

FIG. 3: 039260

The first DSP unit 402 can further include random access memory (RAM) 404 to allow the coefficients of the filters in the DCSP 114 and the complex FIR filter 314 to accept updates and to adapt to the running conditions of the RF transmitter 400. The RAM 404 also functions to store the characteristics of a digital error signal 410, which will be described in greater detail later. The signal processor 402 also includes a clock interface, control logic, and glue logic 406 to interface with a microprocessor 408.

The microprocessor 408 implements the functions of the ACPCE 312. The ACPCE 312 can execute periodically and does not have to operate in real time. Hence, the ACPCE 312 is preferably implemented in a microprocessor such as the 68000 series from Motorola, Inc., or a DSP chip such as the TMS320 series from Texas Instruments Incorporated. A microprocessor core or a DSP core can also be embedded within an ASIC, which can then implement the ACPCE 312 as well as the DCSP 114 and the complex FIR 314 within the same ASIC. Examples of licensable cores include the ARM7 from Advanced RISC Machines, Ltd., the Teak from DSP Group Inc., the Oak from DSP Group Inc., and the ARC from ARC Cores. Of course, the microprocessor 408 or DSP can further include Flash PROMS, ROMs, and other RAMs for program storage and execution. The ACPCE 312 monitors the digital error signal 410 and provides updates to the DCSP 114 and the complex FIR filter 314 to adaptively improve the linearity of the RF transmitter 400 by updating the coefficients of the filters in the DCSP 114 and the complex FIR filter 314.

The remainder of the RF transmitter 400 includes a first, a second, and a third digital-to-analog converter (DAC) 412, 414, 416, an RF modulator/up-converter 418, an RF power amplifier 420, a coupler 422, an RF down-converter 424, a combiner 426, and an analog-to-digital converter 428.

The signal processor 402 can be configured to accept either a digital IF signal or a digital IQ baseband signal as an input signal 430. The DCSP 114 within the signal processor 402 predistorts the input signal 430. As shown in Figure 4, the signal processor 402 provides the first and the second DACs 412, 414 with predistorted I and Q signals 432, 434. In one embodiment, the first and the second DACs 412, 414 are 14-bit DACs that convert digital I and Q signals to analog I and Q signals 436, 438 at the rate of 125 MHz. The RF modulator/up-converter 418 receives a local oscillator signal

440 and directly modulates the analog I and Q signals 436, 438 to the carrier frequency. The RF power amplifier 420 amplifies a modulated output 442 of the RF modulator/up-converter 418.

5 The RF down-converter 424 receives a sample 444 of the output of the RF power amplifier 420 from the coupler 422. In one embodiment, the RF down-converter 424 mixes the sample 444 with the same local oscillator signal 440 used by the RF modulator/up-converter 418.

10 A down-converted output 446 of the RF down-converter 424 is applied to an input of the combiner 426. An output 448 of the third DAC 416 provides the other input of the combiner 426. The signal processor 402 and the third DAC 416 delay by time τ , amplitude scale by factor α , and phase shift by angle Φ , the output 448 of the third DAC 416 with respect to the input signal 420. In one embodiment, the third DAC 416 is a 14-bit DAC that converts data at the rate of 125 MHz. The combiner 426 combines the output 448 of the third DAC 416 with the down-converted output 446
15 such that the main signal component of the down-converted output 446 is reduced in magnitude. If $V_m(t)$ represents the digital input signal 430, the analog output 448 of the third DAC 416 can be represented as:

$$\alpha e^{j\phi} V_m(t - \tau)$$

20 The combining of the analog output 448 of the third DAC 416 with the down-converted output 446 advantageously reduces the main signal component of the down-converted output 446 and allows relatively more of the input range of the ADC 428 to capture the error signal component of the down-converted output 446. In one embodiment, the ADC 428 is a 12-bit Flash ADC that samples an analog error signal output 452 of the combiner 426 at a rate of 125 MHz. The output of the ADC 428 is the
25 digital error signal 410, which is eventually used by the microprocessor 408, which implements the ACPCE 312, to update the coefficients of the DCSP 114 and the complex FIR filter 314 of the signal processor 402.

30 The signal processor 402 can further include a control / Radio Resource Management Entity (RRME) interface 454 to initiate predistortion, configure the frequencies of conversion, configure the number of bits of ADC and DAC conversion, and the like.

In one embodiment, the intended bandwidth of the RF transmitters 300, 400 does not extend substantially beyond one octave of the carrier frequency, i.e., twice the carrier frequency, to avoid the second harmonic of the carrier frequency.

5 Embodiments of the present invention more efficiently quantize the error signals of the outputs of the RF transmitters 300, 400. The more efficient utilization of an ADC used to sample error in an down-converted signal allows an ADC with the same number of bits to quantize the error signal in smaller steps and improve the sensitivity of the RF transmitters 300, 400 to nonlinearities. The enhanced sensitivity can be used to provide more accurate updates to the DCSP 114 and thereby improve the linearity of the RF
10 transmitters 300, 400. The improved linearity can be used, for example, to increase the symbol rate or increase the power of the RF transmitters 300, 400. The more efficient utilization of the analog-to-digital converters also allows the use of a less expensive ADC with a reduced number of quantization bits.

15 Various embodiments of the present invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention as defined in the appended claims.